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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/692,606	10/19/2000	Jack Oon Chu	YOR920000334US1	7913
23389	7590	07/26/2004	[REDACTED]	EXAMINER
				KIELIN, ERIK J
			[REDACTED]	ART UNIT
				PAPER NUMBER
				2813

DATE MAILED: 07/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/692,606	CHU ET AL.	
	Examiner	Art Unit	
	Erik Kielin	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 26 May 2004.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-19 and 21-42 is/are pending in the application.
- 4a) Of the above claim(s) 2-5,7,8,11-17 and 24-42 is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1,6,9,10,18,19 and 21-23 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 04 May 2004 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 4 May 2004 has been entered.

Drawings

2. The drawings were received on 4 May 2004. These drawings are acceptable.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1, 9, 10, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6,521,041 B2 (**Wu et al.**) in view of US 6,328,796 B1 (**Kub et al., Kub '796, hereafter**) and further in view of US 4,826,787 (**Muto et al.**).

Wu discloses a method of preparing a relaxed SiGe layer on an insulator and a SiGe/Si heterostructure comprising the steps of forming a graded $\text{Si}_{1-x}\text{Ge}_x$ epitaxial layer **1004** on a first single crystalline semiconductor substrate **1002** (col. 1, lines 9-10; Fig. 10);

forming a relaxed $\text{Si}_{1-y}\text{Ge}_y$ epitaxial layer **1006** (col. 13, lines 63-64; col. 8, lines 40-48) over said graded $\text{Si}_{1-x}\text{Ge}_x$ layer;

selecting a second substrate **1010**, said second substrate with or without an insulator **1012**, and

bonding said top surface of said relaxed $\text{Si}_{1-y}\text{Ge}_y$ epitaxial layer on said first substrate to the top surface of said second substrate, said step of bonding including the step of annealing to form sufficiently strong bonds across the bonding interface to form a single mechanical structure (Fig. 10). (See also col. 13, line 63 to col. 14, line 23.)

Further regarding claim 1 and claim 10, **Wu** does not indicate whether or not the surface of the relaxed $\text{Si}_{1-y}\text{Ge}_y$ epitaxial layer **1006** is smoothed to provide a surface roughness in the range from about 0.3 nm to about 1 nm root mean square (RMS) using chemical mechanical planarization (CMP) --as further limited by instant claim 10-- prior to bonding, or that the second substrate **1010** with or without an insulator **1012** has a surface roughness in the range from about 0.3 nm to about 1 nm RMS prior to bonding.

Kub '796 teaches that in order to obtain direct bonding between substrates, that the bonding surfaces must have a RMS surface roughness of less than 1 nm and can be obtained by polishing (col. 4, lines 4-8) and that such polishing is known in the art to be chemical mechanical polishing (col. 3, lines 30-32).

It would have been obvious for one of ordinary skill in the art, at the time of the invention to smooth the relaxed $\text{Si}_{1-y}\text{Ge}_y$ epitaxial layer **1006** of Wu using CMP and to provide a surface roughness on the bonding surface of the second substrate **1012** each of less than 1 nm, in order to ensure bonding, as taught by **Kub '796**.

Wu does not teach using an intermediate agent layer selected from the group consisting of W (tungsten) and Ti (titanium) may be used to enhance the bonding interface.

Kub '796 also teaches (1) it is known in the art to use an intermediate agent layer including, *inter alia*, a metal or a metal silicide, said intermediate agent layer having been polished to have a RMS surface roughness less than 1 nm (col. 4, lines 13-17; col. 7, lines 17-21) to aid the bonding between substrates, and (2) it is known in the art that “[m]aterials such as silicon and germanium that melt during a bonding process and **react with the substrate material** can be used to bond two SiC substrates together” (col. 4, lines 35-37). between the metal and the crystalline substrate during the bonding step, thereby forming a silicide, as indicated in **Kub '796** (col. 4, lines 24-34; col. 6, lines 51-53 and col. 7, lines 6-21).

It would have been obvious for one of ordinary skill in the art, at the time of the invention to use a polished, intermediate agent layer of a metal or metal silicide at the bonding interface between the substrates in **Wu**, in order to aid the bonding of the substrates, as taught by **Kub '796**.

Then the only difference is that **Kub '796** does not indicate the identity of the metals or metal silicides used to form the metal silicide interface or that the silicide formed during the annealing step to bond. Note, as stated above, that **Kub '796** does teach that it is known in the art to generate bonding between substrates by reacting the intermediate agent layer with the substrate material (col. 4, lines 35-37).

Muto teaches a method of bonding silicon-based semiconductor wafers together by depositing a metal, such as zirconium (or other group IVa and Va metals), on one of

the silicon-based substrates, bringing the wafers together, and then annealing to bond the wafers by the production of metal silicide (Abstract; all Figures). **Muto** also states,

“Advantages of this adhesion method are: the process is carried out at approximately 650 °C, which does not harm fabricated devices; the adhesion withstands temperatures of 1000 °C which are used for fabricating devices; and the processing does not require strict control of the surface conditions.” (Abstract)

It would have been obvious for one of ordinary skill in the art, at the time of the invention to perform the substrate bonding of **Kub '796** by forming the silicide intermediate agent layer during annealing to bond the wafers, as taught by **Muto**, (1) because **Kub '796** suggests using a metal silicide without indicating how the silicide is fabricated, such that one of ordinary skill would be motivated to find how to make the silicide bonding layer; (2) **Kub '796** suggests bonding by reaction of the intermediated agent layer with the substrate, e.g. reaction of metal with silicon substrate to make the metal silicide (col. 4, lines 35-37); (3) **Muto** teaches the method advantageously is a low temperature process which spares damage to semiconductor devices and relaxes the strict control over the surface conditions; and (4) manufacturing the silicide during annealing would circumvent the step of depositing the metal silicide first prior to the bonding anneal and therefore would save time. One of ordinary skill would be motivated to gain the advantages taught by **Muto**.

Finally, it would be obvious to use the combined teachings of **Kub '796** and **Muto** to form the intermediate agent layer of **Wu** to gain the benefits of improved bonding taught by **Kub '796** and **Wu**, as already expressed above.

Regarding claim 9, **Wu** discloses that the first substrate **1002** is selected from the group consisting of Si, SiGe, SiGeC, SiC, GaAs, or InP.

Regarding claim 18, **Wu** discloses that the second substrate **1010** is selected from the group consisting of Si, SiGe, SiGeC, SiC, GaAs, InP, sapphire, glass, quartz, LiNbO₃, and PLZT.

Regarding claim 19, **Wu** discloses that said the top surface of said first Si_{1-y}Ge_y relaxed layer **1006** on said first substrate **1002** is brought into intimate contact with said top surface of an insulator layer **1012** on said second substrate **1010**.

5. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Wu** in view of **Kub '796** and **Muto** as applied to claim 1 above, and further in view of US 5,906,951 (**Chu et al.**).

The prior art of **Wu**, as explained above, discloses each of the claimed features except for providing the thickness low-defect relaxed Si_{1-y}Ge_y layer on said second substrate to be in the range from about 50 nm to about 1000 nm as determined by the layer structure formed on said first substrate.

Chu teaches a very similar method to that in **Wu** of using a relaxed silicon-germanium layer as an etch stop and teaches that the thickness may be from 200 nm to 1000 nm (col. 2, lines 61-67; Fig. 3).

It would have been obvious for one of ordinary skill in the art, at the time of the invention to use the thickness of 200 nm to 1000 nm as the relaxed Si_{1-y}Ge_y layer of **Wu**, because **Wu** is silent to the thickness, such that one of ordinary skill must determine the appropriate thickness, and using a known thickness for an etch stop in a similar method would dramatically reduce the experimentation required to determine the proper thickness. With this in mind, the choice of thickness range is *prima facie* obvious without

showing that the claimed range achieves unexpected results relative to the prior art range. See *In re Woodruff*, 16 USPQ2d 1935, 1937 (Fed. Cir. 1990). See also *In re Boesch*, 205 USPQ 215 (CCPA) (discovery of optimum value of result effective variable in known process is ordinarily within skill of art) and *In re Aller*, 105 USPQ 233 (CCPA 1955) (selection of optimum ranges within prior art general conditions is obvious).

6. Claims 1, 9, 10, 19, and 21-23 are rejected under 35 U.S.C. 103(a) as being

unpatentable over US 6,573,126 B2 (**Cheng et al.**) in view of **Kub '796** and **Muto**.

Cheng discloses a method of preparing a relaxed SiGe layer on an insulator and a SiGe/Si heterostructure comprising the steps of

forming a graded $\text{Si}_{1-x}\text{Ge}_x$ epitaxial layer **102** on a first single crystalline semiconductor substrate **100** (Fig. 1A);

forming a relaxed $\text{Si}_{1-y}\text{Ge}_y$ epitaxial layer **104** over said graded $\text{Si}_{1-x}\text{Ge}_x$ layer (Fig. 1A);

smoothing the surface of said relaxed $\text{Si}_{1-y}\text{Ge}_y$ epitaxial layer **104** to provide a surface roughness in the range from about 0.3 nm to about 1 nm root mean square (RMS) using CMP (col. 4, last paragraph) --as further limited by instant claim 10;

selecting a second substrate **108**, said second substrate with or without an insulator **106** (Fig. 1B); and

bonding said top surface of said relaxed $\text{Si}_{1-y}\text{Ge}_y$ epitaxial layer on said first substrate to the top surface of said second substrate, said step of bonding including the step of annealing to form sufficiently strong bonds across the bonding interface to form a

single mechanical structure (Fig. 1B). (See also col. 3, lines 28-37; col. 4, lines 20-34; paragraph bridging cols. 4 and 5; col. 5, lines 4-16.)

Cheng does not indicate whether or not the second substrate **108** with or without an insulator **106** has a surface roughness in the range from about 0.3 nm to about 1 nm RMS prior to bonding.

Kub '796 teaches that in order to obtain direct bonding between substrates, that the bonding surfaces must have a RMS surface roughness of less than 1 nm and can be obtained by polishing (col. 4, lines 4-8).

It would have been obvious for one of ordinary skill in the art, at the time of the invention to provide a surface roughness on the bonding surface of the second substrate **106** of less than 1 nm, in order to ensure bonding, as taught by **Kub '796**.

Cheng does not teach using an intermediate agent layer selected from the group consisting of W (tungsten) and Ti (titanium) may be used to enhance the bonding interface.

Then the only difference is that **Kub '796** does not indicate the identity of the metals or metal silicides used to form the metal silicide interface or that the silicide formed during the annealing step to bond. Note, as stated above, that **Kub '796** does teach that it is known in the art to generate bonding between substrates by reacting the intermediate agent layer with the substrate material (col. 4, lines 35-37).

Muto teaches a method of bonding silicon-based semiconductor wafers together by depositing a metal, such as zirconium (or other group IVa and Va metals), on one of the silicon-based substrates, bringing the wafers together, and then annealing to bond the wafers by the production of metal silicide (Abstract; all Figures). **Muto** also states,

“Advantages of this adhesion method are: the process is carried out at approximately 650 °C, which does not harm fabricated devices; the adhesion withstands temperatures of 1000 °C which are used for fabricating devices; and the processing does not require strict control of the surface conditions.” (Abstract)

It would have been obvious for one of ordinary skill in the art, at the time of the invention to perform the substrate bonding of **Kub ‘796** by forming the silicide intermediate agent layer during annealing to bond the wafers, as taught by **Muto**, (1) because **Kub ‘796** suggests using a metal silicide without indicating how the silicide is fabricated, such that one of ordinary skill would be motivated to find how to make the silicide bonding layer; (2) **Kub ‘796** suggests bonding by reaction of the intermediated agent layer with the substrate, e.g. reaction of metal with silicon substrate to make the metal silicide (col. 4, lines 35-37); (3) **Muto** teaches the method advantageously is a low temperature process which spares damage to semiconductor devices and relaxes the strict control over the surface conditions; and (4) manufacturing the silicide during annealing would circumvent the step of depositing the metal silicide first prior to the bonding anneal and therefore would save time. One of ordinary skill would be motivated to gain the advantages taught by **Muto**.

Finally, it would be obvious to use the combined teachings of **Kub ‘796** and **Muto** to form the intermediate agent layer of **Cheng** to gain the benefits of improved bonding taught by **Kub ‘796** and **Wu**, as already expressed above.

Regarding claim 21, **Cheng** discloses that the step of annealing includes thermal treatment cycles to form a strong bond at said bonded interface, said thermal treatment selected from the group consisting of furnace anneal and/or rapid thermal anneal (RTA) (col. 4, lines 20-34; col. 5, lines 51-53).

Regarding claim 23, **Cheng** discloses that the annealing step includes annealing at 600 °C and 850 °C (col. 4, lines 20-34).

7. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Cheng** in view of **Kub '796** and **Muto** as applied to claims 1 and 21 above, and further in view of US 6,153,495 (Kub et al., **Kub '495**, hereafter).

The prior art of **Cheng** in view of **Kub '796**, as explained above, discloses each of the claimed features except for indicating what the annealing ambient is or more specifically that the ambient is selected from the group consisting of air, N₂ and Ar.

Kub '495 teaches that the bonding ambient for bonding a semiconductor layer to an oxide layer may include nitrogen (N₂) and argon (Ar) (col. 6, lines 23-38).

It would have been obvious for one of ordinary skill in the art, at the time of the invention to use an anneal ambient selected from the group consisting of N₂ and Ar, because **Cheng** is silent to the annealing ambient such that one of ordinary skill would use an ambient known for successful wafer bonding, such as that taught in **Kub'495**.

Response to Arguments

8. Applicant's arguments with respect to all pending claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Art Unit: 2813

US 5,387,555 (**Linn et al.**), US 5,569,620 (**Linn et al.**), US 6,118,181 (**Merchant et al.**), and US 6,255,731 (**Ohmi et al.**) each teach bonding silicon-based wafers together by applying a metal to one substrate, contacting the metal with the silicon substrate and then annealing to form a metal silicide that bonds the wafers together.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Erik Kielin whose telephone number is 571-272-1693. The examiner can normally be reached on 9:00 - 19:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Erik Kielin
Primary Examiner
23 July 2004